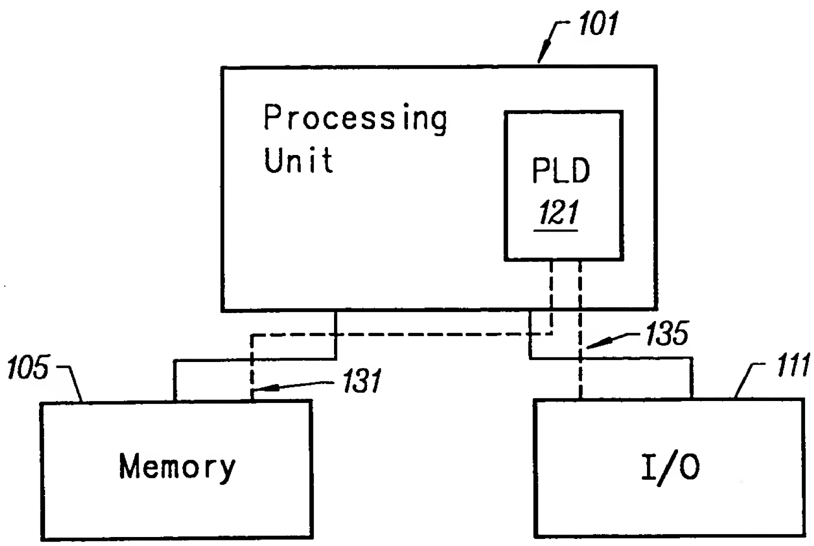
101
Processing Unit
PLD
121
135
105
131
111
Memory
I/O

FIG. 1

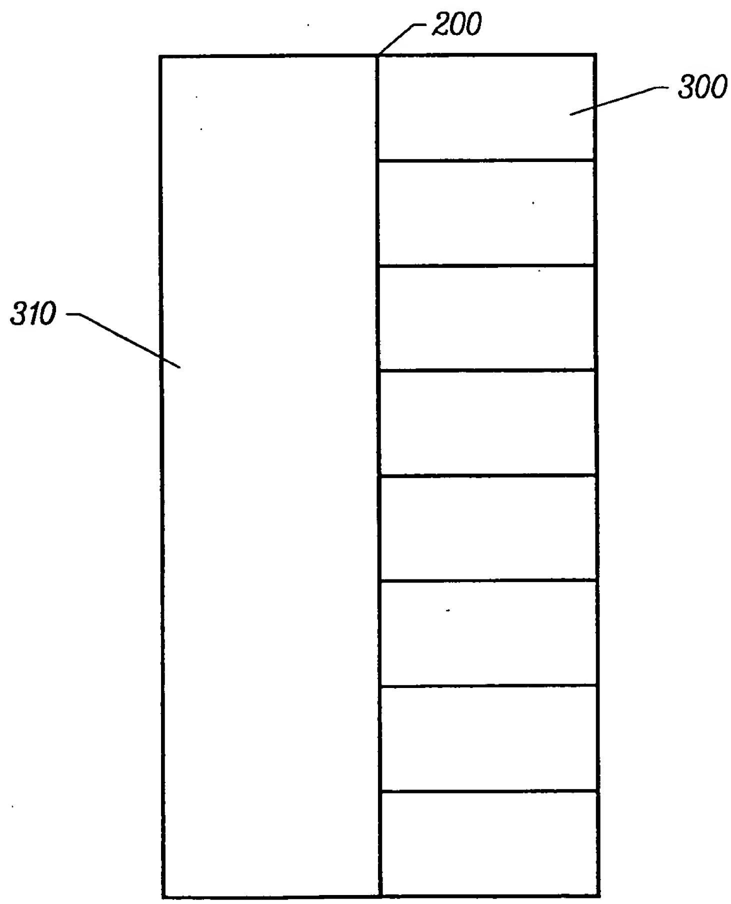
200
300
310

FIG. 3

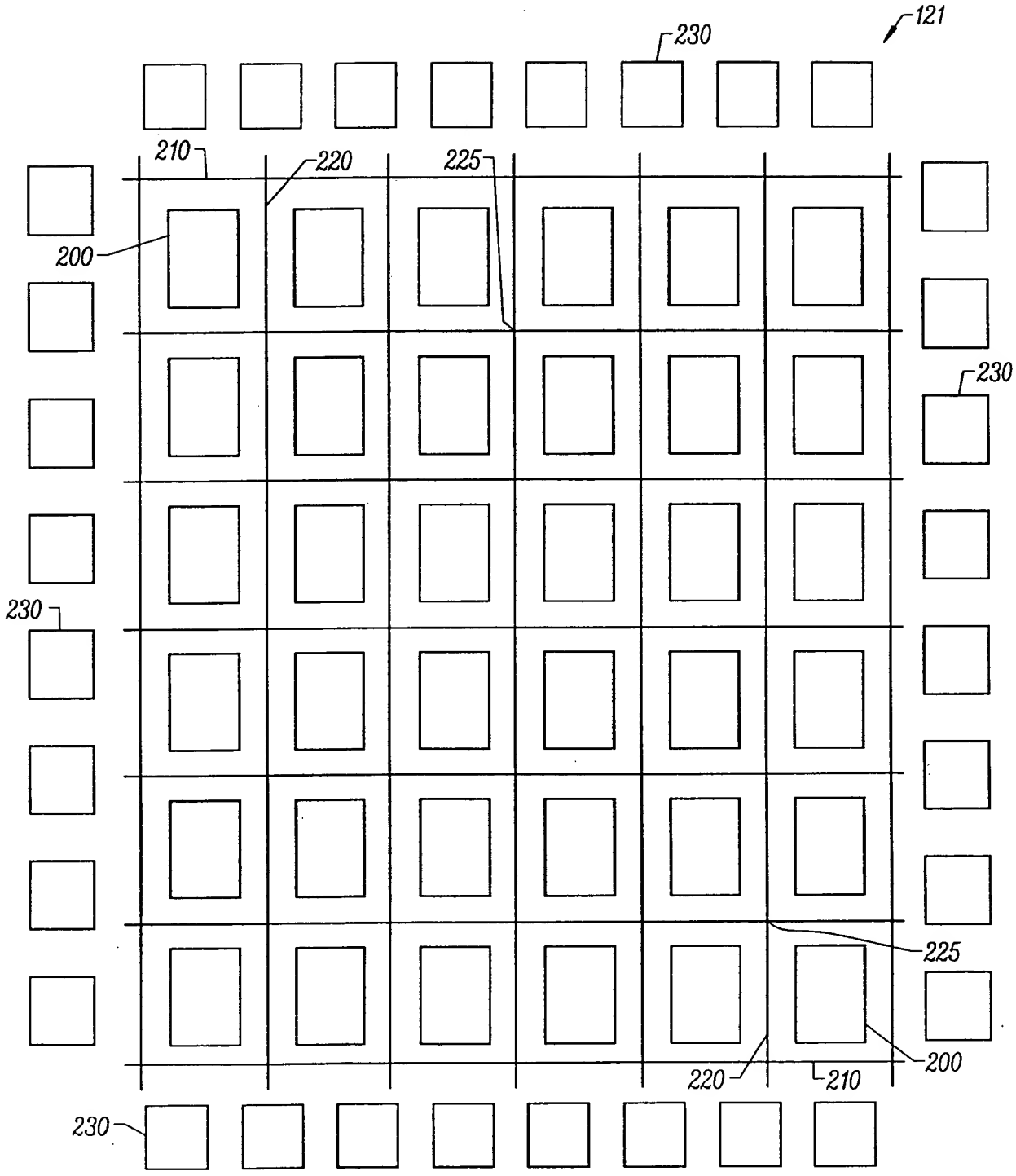

FIG. 2

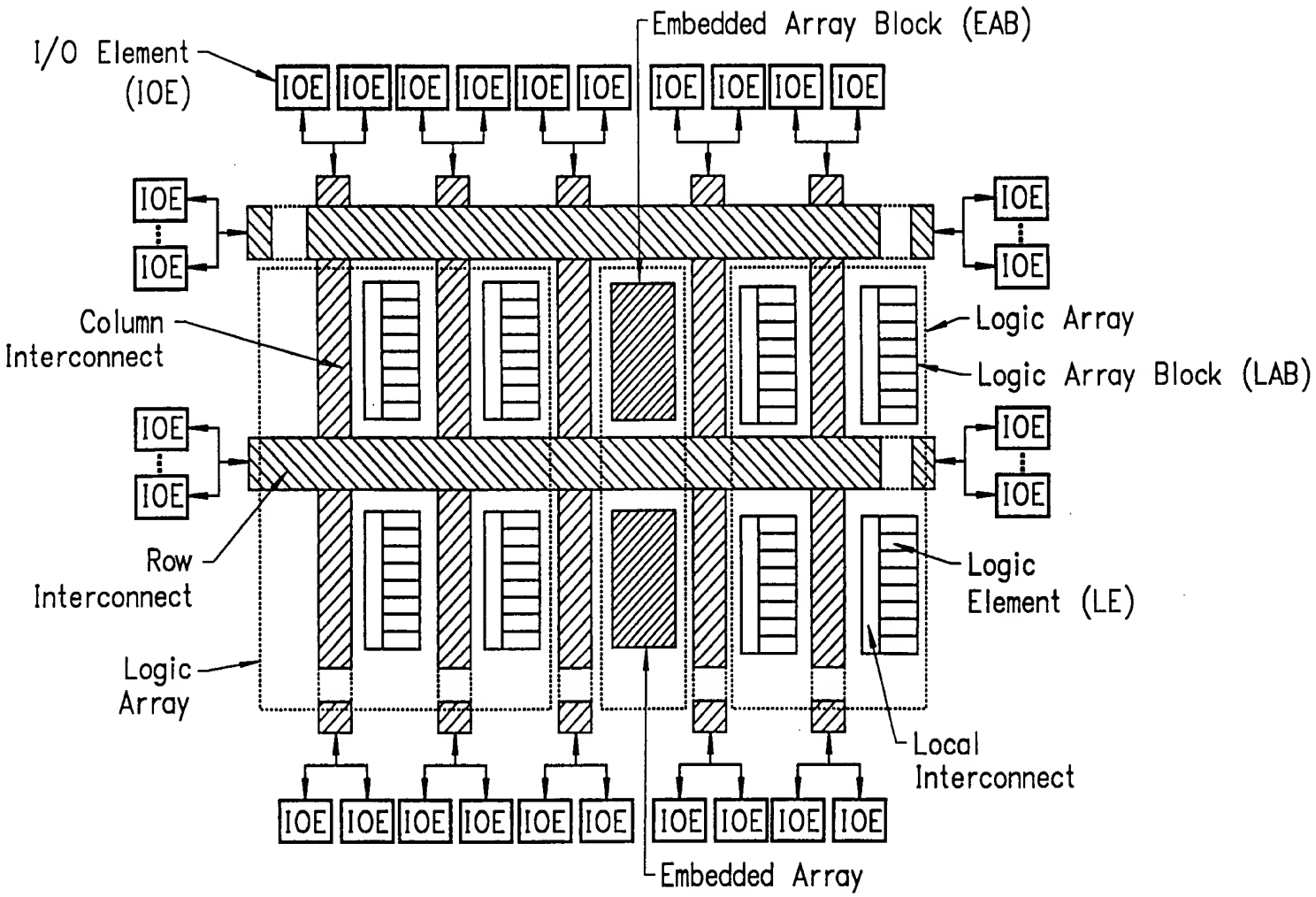

FIG. 4

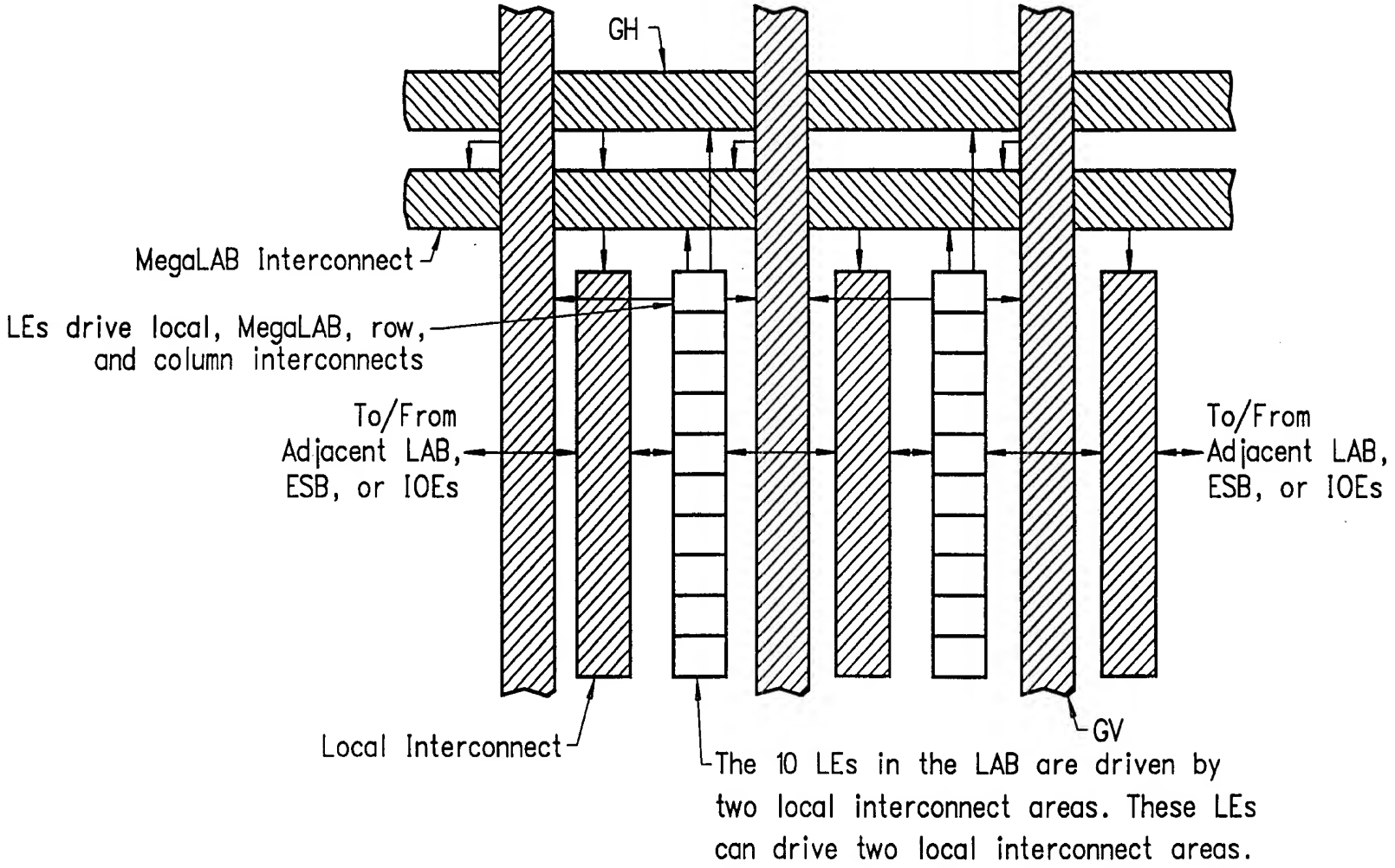

FIG. 5

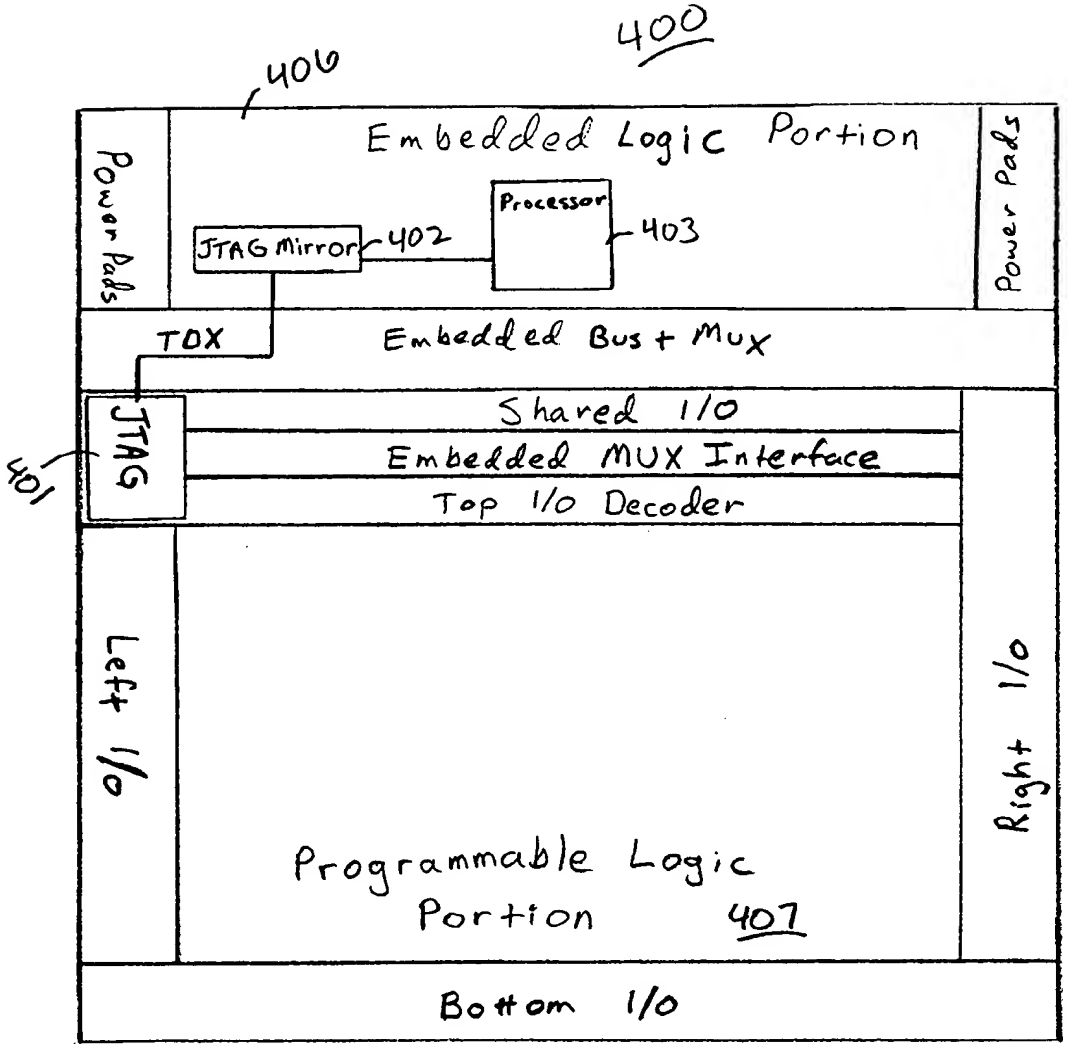
400
406
Embedded Logic Portion
Power Pads
Power Pads
Processor
403
JTAG Mirror
402
TDX
Embedded Bus + MUX
JTAG
401
Shared I/O
Embedded MUX Interface
Top I/O Decoder
Left I/O
Right I/O
Programmable Logic Portion
407
Bottom I/O

FIG. 6

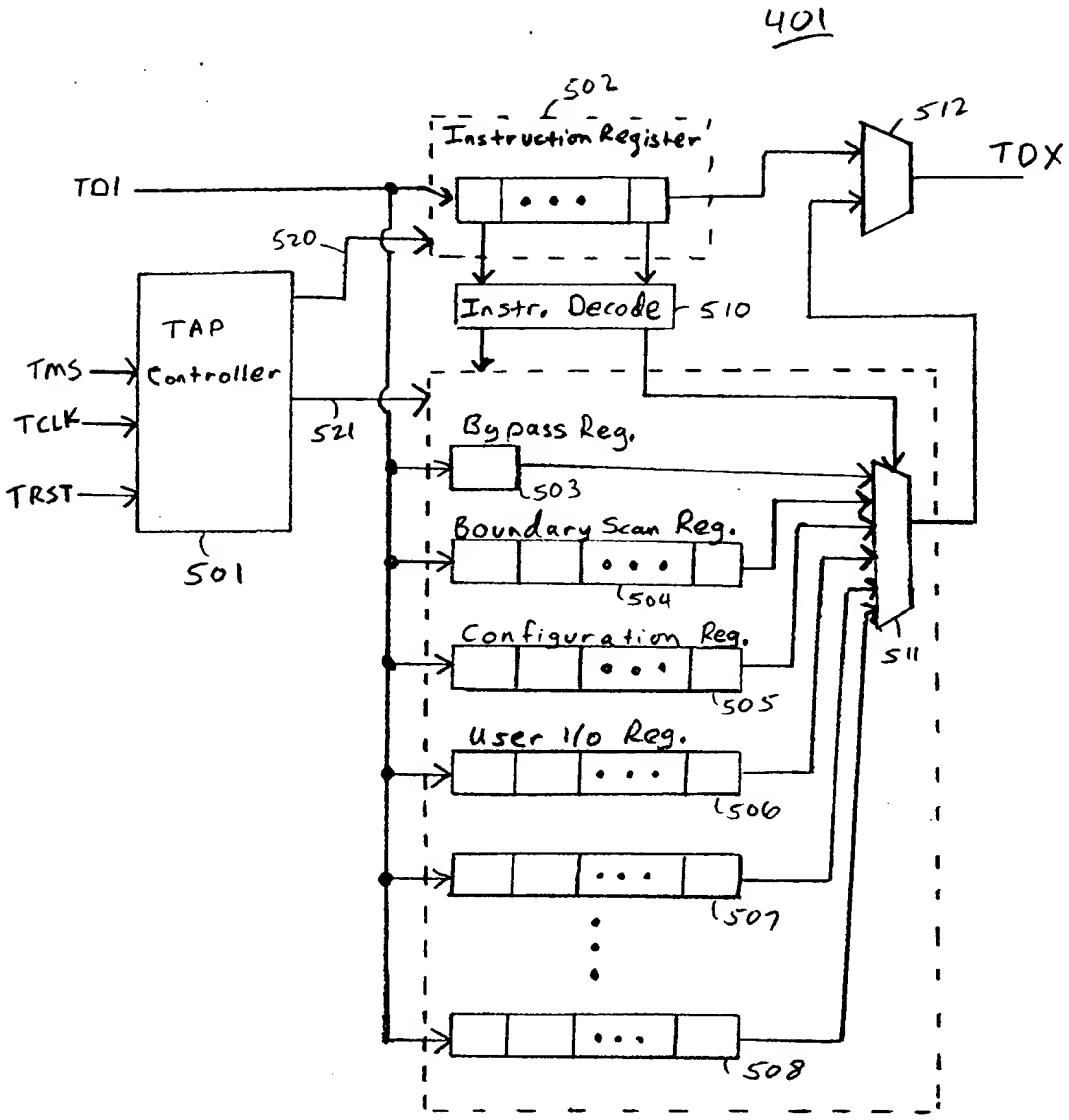
401
502
Instruction Register
512
TDX
TDI
520
TAP
Controller
Instr. Decode
510
TMS
TCLK
TRST
521
501
Bypass Reg.
503
Boundary Scan Reg.
504
Configuration Reg.
505
511
User I/O Reg.
506
507
508

FIG. 7

402

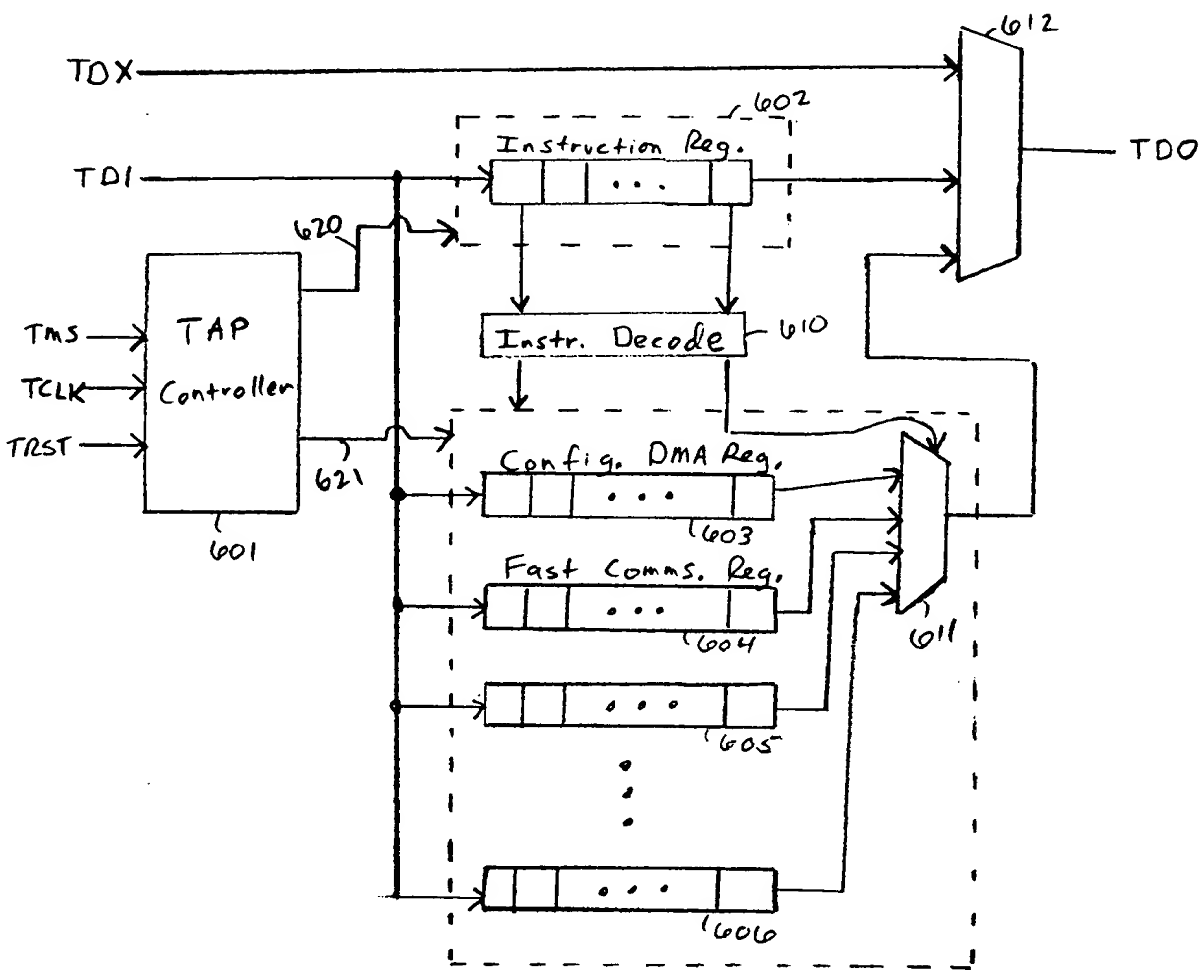

FIG. 8

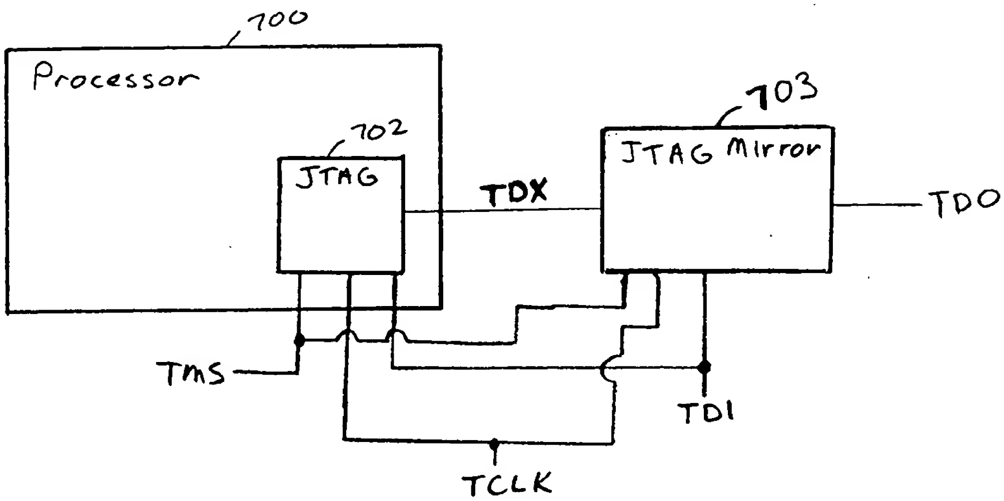

FIG. 9

last bit → 79 ... 0 → first bit

79	78–70	69	68–64	63–32	31–0
WB	0	E	ACTION	ADDRESS	DATA

FIG. 10

31–4	3–2	1	0
0	PC	BE	U

FIG. 11

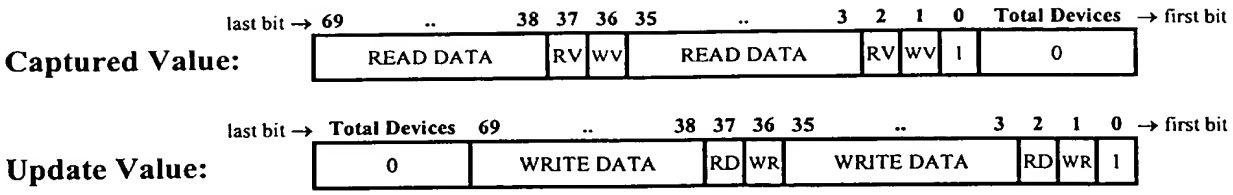

FIG. 12

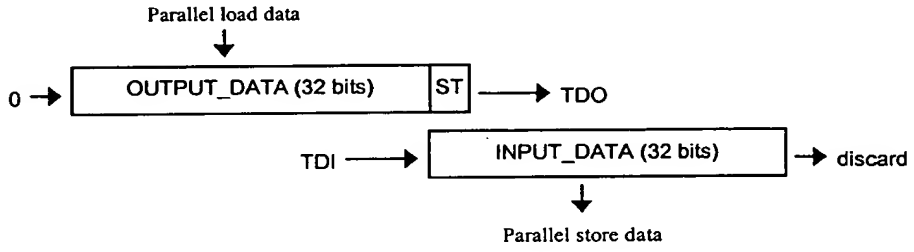

FIG. 13

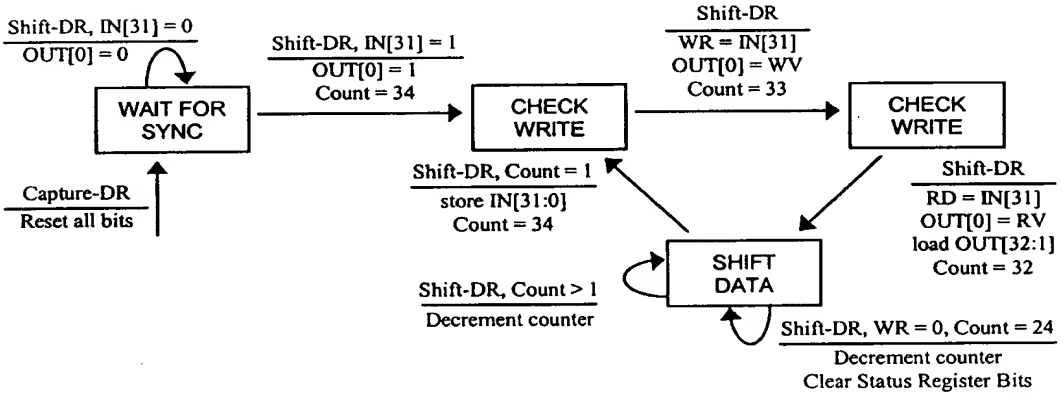

FIG. 14

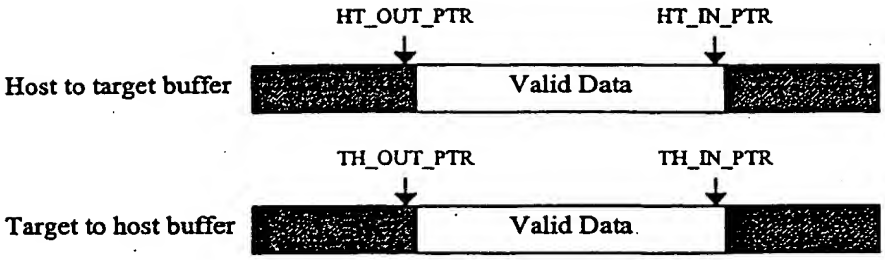

FIG. 15

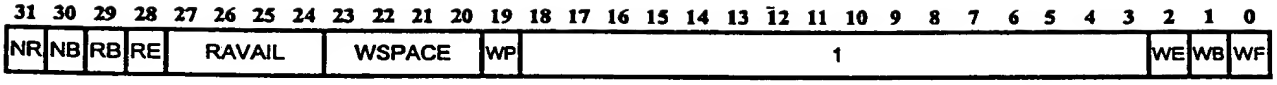

FIG. 16